REMARKS

Claims 1-7 remain pending in the present application. Claims 1-7 have not been amended.

Rejections under 35 U.S.C. §102(e)

The Office has rejected claims 1-7, under 35 U.S.C. §102(e) as allegedly being anticipated by Kishimoto et al. (6,473,321). Applicants respectfully traverse.

To support a rejection of claims 1-7 under 35 U.S.C. Sec. 102(e), the cited reference must disclose every feature in the combination specified in the claims. Kishimoto et al. does not disclose each of the features of Applicants' claimed semiconductor memory device.

It is Applicants' opinion that Kishimoto et al. does not disclose a memory cell array comprising a two-value memory region and a multi-value memory region having a sense amplifier section common to data read of the two-value memory region and data read of the multi-value memory regions as specified in Applicants' claims. Nowhere does Kishimoto et al. disclose two bits of write data being stored in a memory region. Kishimoto et al. discloses that the data converter **20** of Fig. 9 of Kishimoto et al. converts every two bits of write data entered from outside into four-value data (column 14 lines 20-23). Data converter **20** has four lines emerging from its center portion that feed the four bits of information to each of MAT-U and MAT-D. Each of MAT-U and MAT-D of Kishimoto et al.'s memory array **10** is configured as a four-bit memory array (see Fig. 9 of Kishimoto et al.). It does not appear from Kishimoto et al.'s disclosure that Kishimoto et al. stores any information having only two bits. It appears that all two-bit information from outside is immediately converted into four-bit data and is stored as such in MAT-U and MAT-D.

Further, Fig. 9 of Kishimoto et al. discloses that each of MAT-U and MAT-D has separate amplifiers. MAT-D utilizes the four Mat Amplifiers depicted beneath Kishimoto et al.'s Data Converter **20**, and MAT-U utilizes the four Mat Amplifiers depicted above Kishimoto et al.'s

Data Converter 20. Kishimoto et al. therefore does not disclose that both MAT-U and MAT-D use an amplifier common to both memory regions.

Since Kishimoto et al. does not disclose a semiconductor memory device having all of the features specified in Applicants' claim 1, Kishimoto et al. cannot anticipate claim 1 under 35 U.S.C. Sec. 102(e). Dependent claims 2-7 are patentable over Kishimoto et al. for the same reasons.

CONCLUSION

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952 referencing docket no. 299002056800. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

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Respectfully submitted,

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